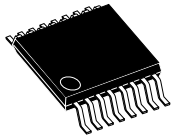
STLVDS31

High speed differential line drivers

Feature summary

- Meets or exceeds the requirements of ansi TIA/EIA-644 standard
- Low voltage differential signaling with typical output voltage of 350mV and a 100Ω load
- Typical output voltage rise and fall times of 750ps (400mbps)
- Typical propagation delay times of 1.7ns
- Operates from a single 3.3V supply
- Power dissipation 25mW typical per driver at 200MHz
- Driver at high impedance when disabled or with V_{CC} = 0V
- Pin compatible with the AM26LS31, SN65LVD31
- Low voltage TTL (LVTTL) logic input levels



TSSOP

Description

The STLVDS31 is a quad differential line drivers that implements the electrical characteristics of low voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds and allows operations with a 3.3V supply rail. Any of the four current mode drivers will deliver a minimum differential output voltage magnitude of 247mV into a 100Ω load when enabled.

The intended application of this device and signalling technique is for point-to-point baseband data transmission over controlled impedance media approximately 100Ω. The transmission media may be printed circuit board traces, backplanes or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and noise coupling to the environment.

The STLVDS31 is characterized for operation from -55°C to 125°C.

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Order code

Part number	Temperature Range	Package	Comments
STLVDS31BTR	-55 to 125 °C	TSSOP16 (Tape & Reel)	2500 parts per reel

Contents

1 Pin configuration

Figure 1. Pin connections and functional diagram

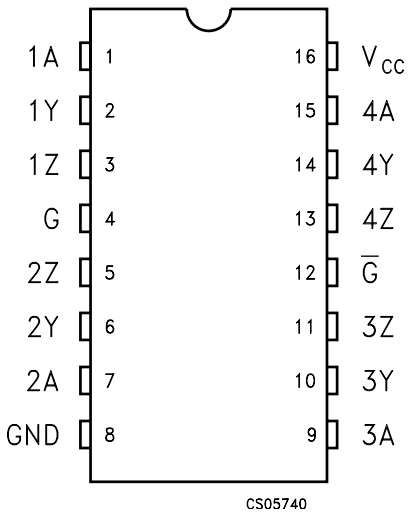


Table 1. Pin description

Pin n°	Symbol	Name and function
1, 7, 9, 15	1A to 4A	Driver inputs
2, 6, 10, 14	1Y to 4Y	Driver outputs
3, 5, 11, 13	1Z to 4Z	Driver outputs
4	G	Enable
12	G	Enable
8	GND	Ground
16	V_{CC}	Supply voltage

Figure 2. Logic diagram and logic symbol

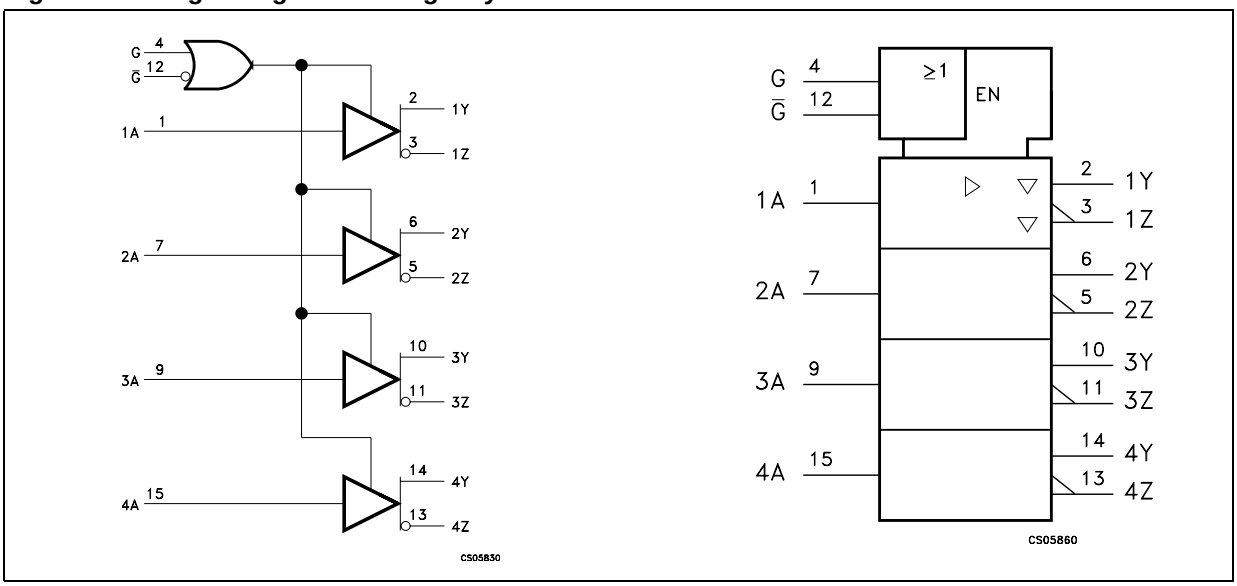


Table 2. Truth table for receiver

$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100mV$	H
$-100mV < V_{ID} < 100mV$	?
$V_{ID} \leq -100mV$	L
OPEN	H

Table 3. Truth table

Input	Enables		Outputs	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
OPEN	H	X	L	H
OPEN	X	L	L	H

L=Low level, H=High Level, X=Don't care, Z= High Impedance

2 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (1)	-0.5 to 4.6	V
V_I	DC Input Voltage	-0.5 to (V_{CC} + 0.5)	V
T_{stg}	Storage Temperature Range	-65 to +150	°C

1. All voltages except differential I/O bus voltage, are with respect to the network ground terminal.

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	HIGH Level Input Voltage	2.0			V
V_{ILI}	LOW Level Input Voltage			0.8	V
T_A	Operating Temperature Range	-40		85	°C

3 Electrical characteristics

Table 6. Electrical characteristics
(Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25°C, and V_{CC} = 3.3V).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_{OD}	Differential Output Voltage	R_L = 100Ω, Fig. 2	247	350	454	mV
ΔV_{OD}	Change in Differential Output Voltage Between Logic State		-50		50	mV
$\Delta V_{OC(SS)}$	Change in Steady-state Common Mode Output Voltage Between Logic State	Fig. 3	1.125	1.2	1.375	V
$V_{OC(SS)}$	Steady-state Common Mode Output Voltage	Fig. 3	-50		50	mV
$V_{OC(PP)}$	Peak to Peak Common mode Output Voltage			80	150	mV
I_{CC}	Supply Current	V_{IN} = 0.8V or 2V, Enabled, No Load		11.5	20	mA
		V_{IN} = 0.8V or 2V, Enabled, R_L = 100Ω		25	35	mA
		V_{IN} = 0 or V_{CC}, Disabled		0.3	1	mA
I_{IH}	High Level Input Current	V_{IH} = 2V		4	20	µA
I_{IL}	Low Level Input Current	V_{IL} = 0.8V		0.6	10	µA
I_{SC}	Short Circuit Output Current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0V		6.1	-24	mA
		V_{OD} = 0			± 12	mA
I_{OZ}	High Impedance Output Current	V_O = 0 or 2.4V			± 1	µA
I_{CS}	Cold Spare Leakage Current	V_I = 3.6V, V_{DD} = 0V			±20	µA
I_{OFF}	Power OFF Output Current	V_{CC} = 0V$_O$ = 2.4V			± 1	µA
C_{IN}	Input Capacitance			3		pF

Table 7. Switching characteristics
(Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25°C, and V_{CC} = 3.3V).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay Time, Low to High Output	R_L = 100Ω, C_L = 10pF Fig. 2	0.5	1.4	2	ns
t_{PHL}	Propagation Delay Time, High to Low Output		1	1.7	2.5	ns
t_r	Differential Output Signal Rise Time		0.4	0.5	0.6	ns
t_f	Differential Output Signal Fall Time		0.4	0.5	0.6	ns
$t_{sk(P)}$	Pulse Skew ($\|t_{THL} = t_{TLH}\|$)			0.3	0.6	ns
$t_{sk(O)}$	Channel to Channel Output Skew (1)			0	0.3	ns
t_{PZH}	Propagation Delay Time, High Impedance to High Level Output	Fig. 4		5.4	15	ns
t_{PZL}	Propagation Delay Time, High Impedance to Low Level Output			2.5	15	ns
t_{PHZ}	Propagation Delay Time, High Level to High Impedance Output			8.1	15	ns
t_{PLZ}	Propagation Delay Time, Low Level to High Impedance Output			7.3	15	ns

1. $t_{sk(O)}$ is the maximum delay time difference between drivers on the same device.

RS-232 IN to TTL-CMOS OUT (from 50% to 50%).

4 Typical characteristics

Figure 3. Voltage and current definitions

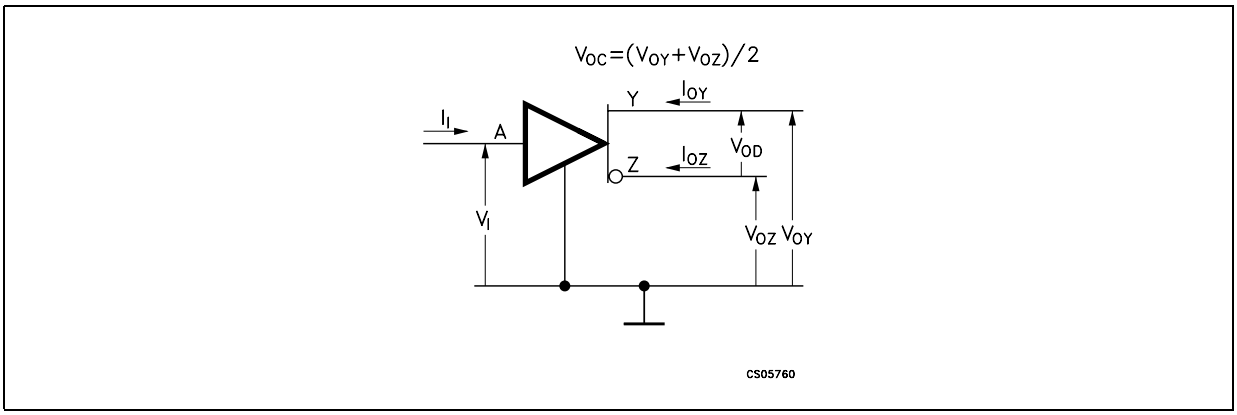
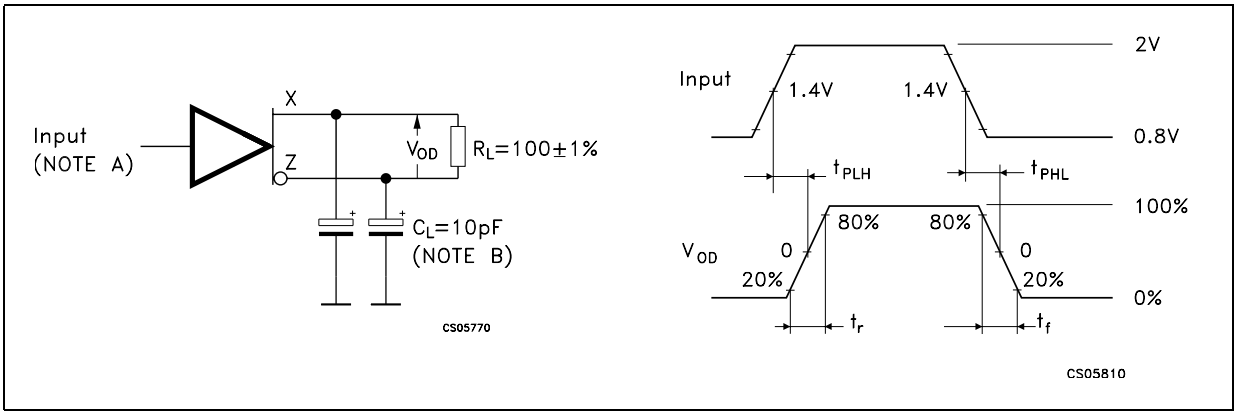


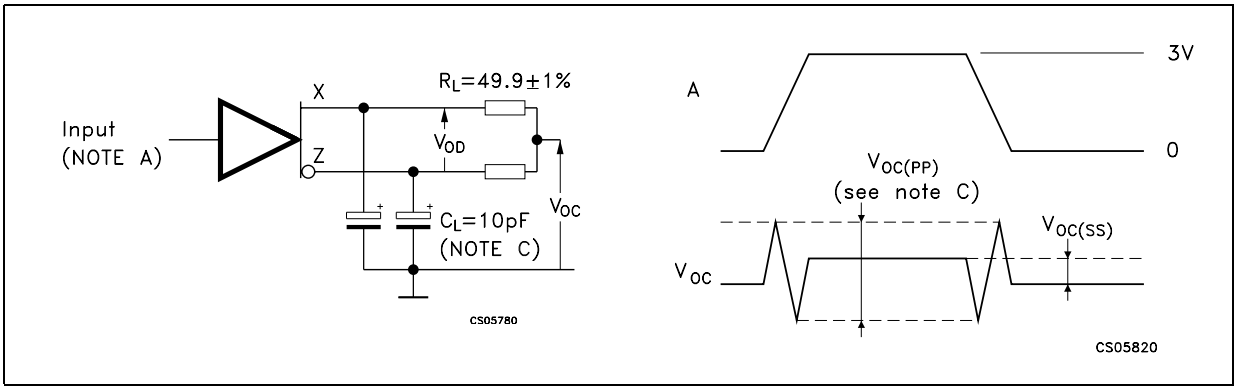
Figure 4. Test circuit, timing and voltage definitions for differential output signal



Note A: All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, pulse repetition rate (PRR) = 50Mpps, pulse width = 10 ± 0.2ns.

Note B: C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.

Figure 5. Test circuit and definitions for the driver common mode output voltage

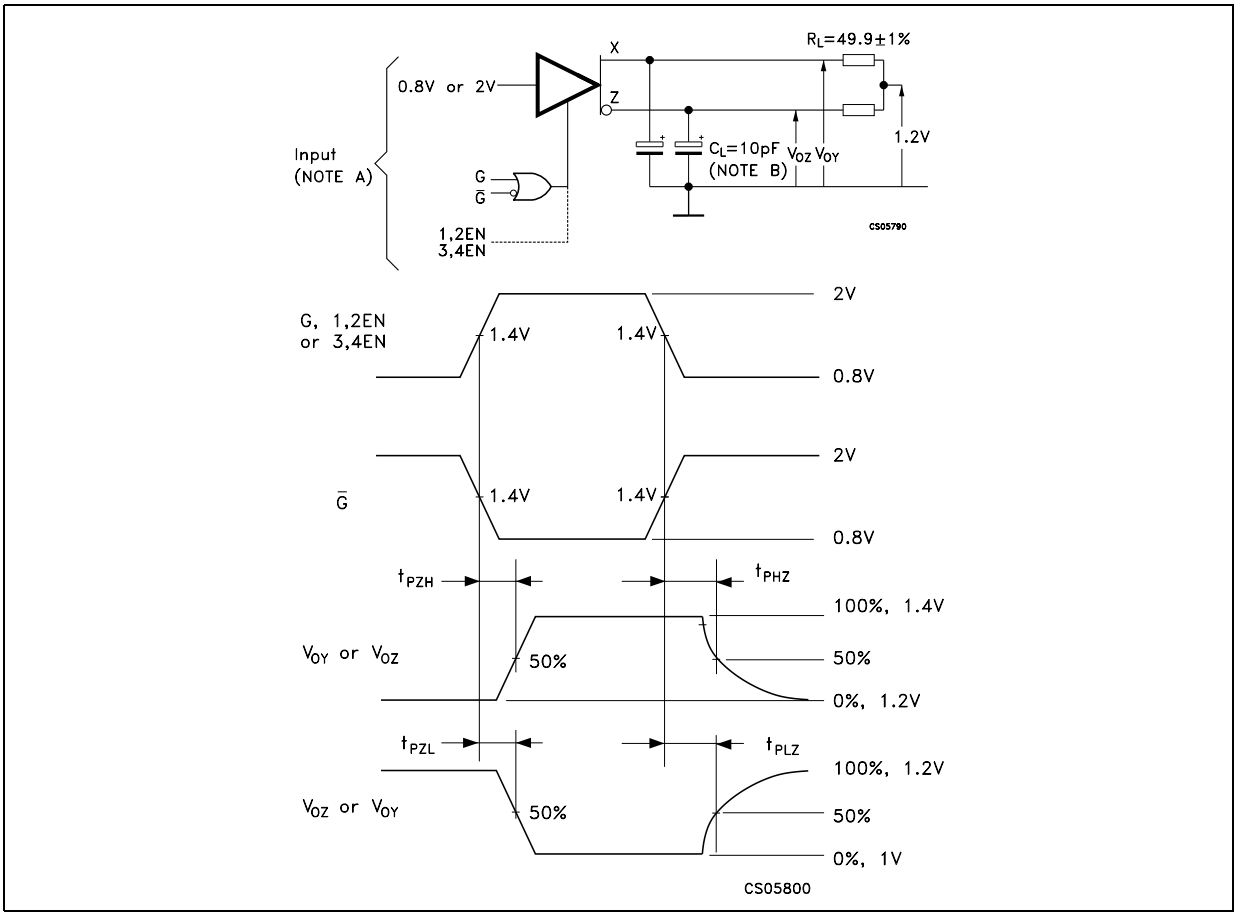


Note A: All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, pulse repetition rate (PRR) = 50Mpps, pulse width = 10 ± 0.2ns.

Note B: C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T

Note C: The measurement of VOC(PP) is made on test equipment with a -3dB bandwidth of at least 300MHz.

Figure 6. Enable and disable time test circuit and waveform



Note A: All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, pulse repetition rate (PRR) = 0.5Mpps, pulse width = 500 ± 10ms.

Note B: C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.

5 Typical performance characteristics

(Unless otherwise specified T_J = 25°C)

Figure 7. Supply Current vs Temperature

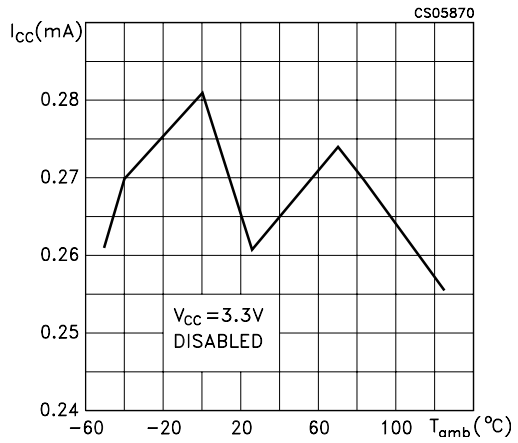


Figure 8. Supply Current vs Temperature

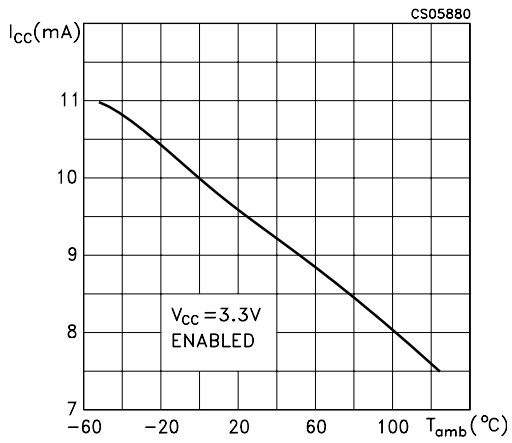


Figure 9. Propagation Delay Enable to Output

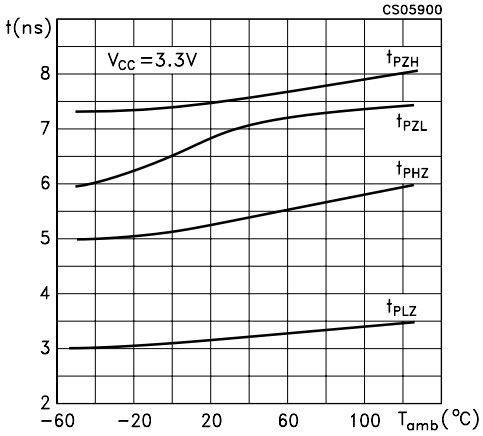


Figure 10. Propagation Delay time

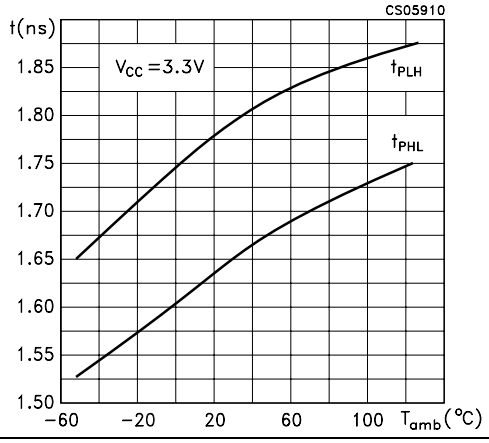
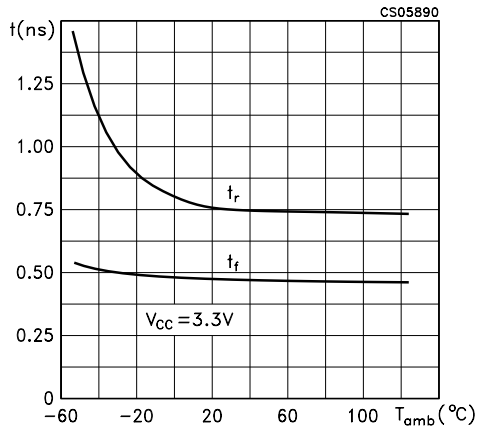


Figure 11. Differential Output Signal

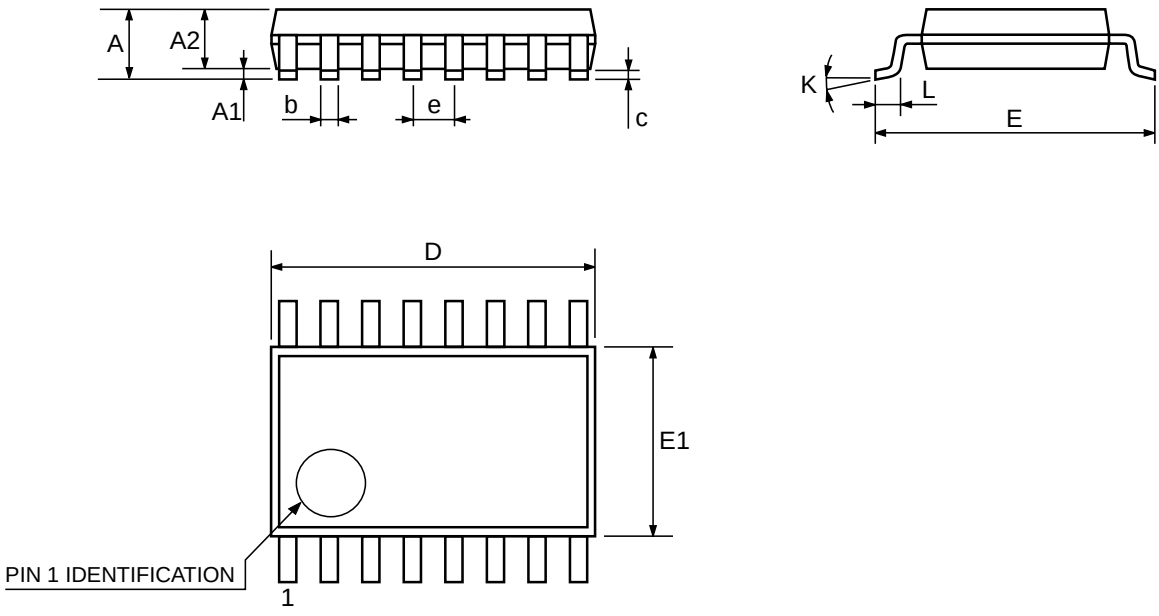


6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

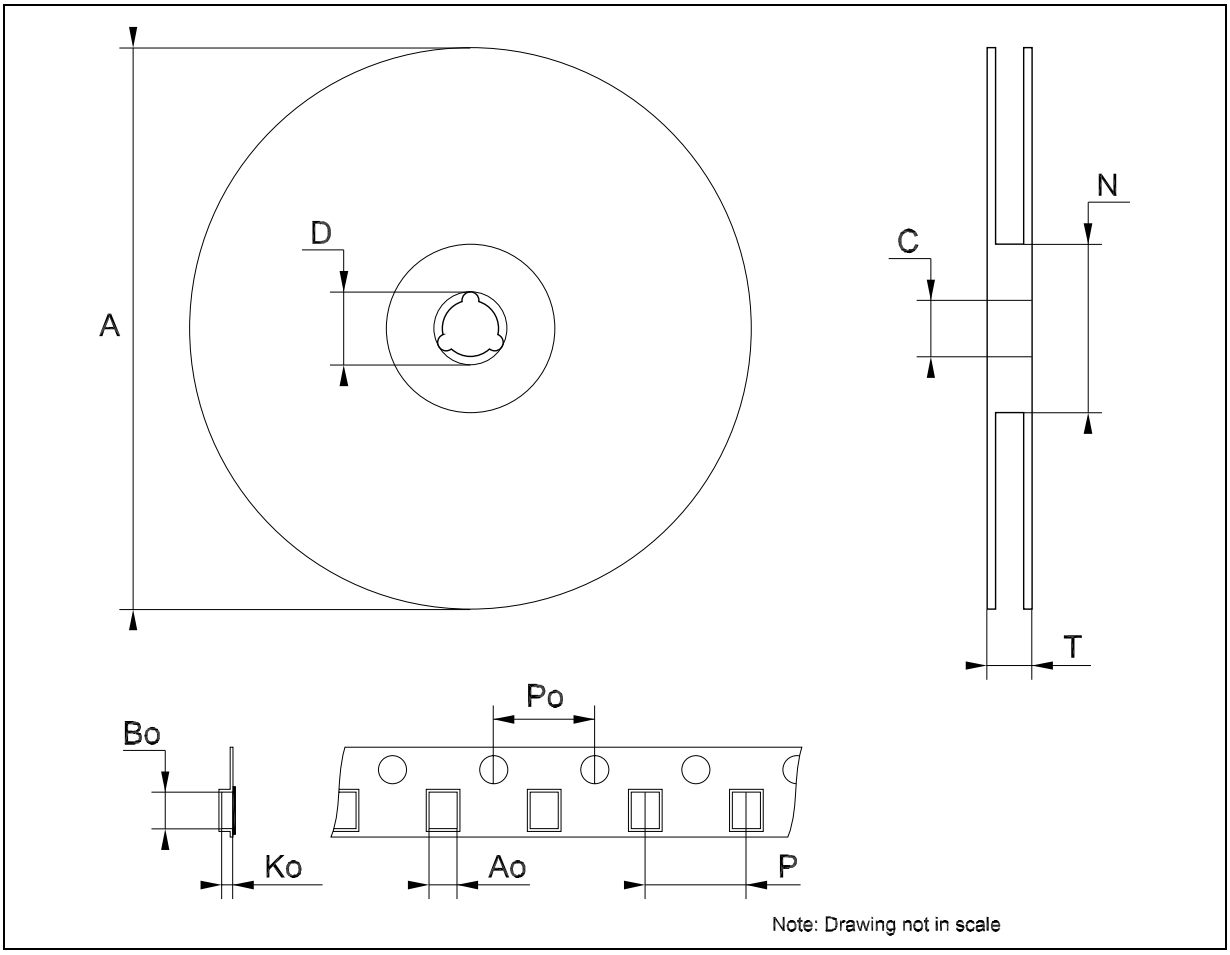
TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

7 Revision history

Table 8. Revision history

Date	Revision	Changes
28-Mar-2006	5	Order codes has been updated and new template.

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